

WHAT IS CLAIMED IS:

- 1 1. A method of fabricating a lead frame for a semiconductor device
2 package, the method comprising:
3 providing a first metal layer;
4 patterning a mask over the first metal layer to reveal exposed regions;
5 electroplating a metal over the exposed regions;
6 removing the mask; and
7 encapsulating at least a portion of the first metal layer and the electroplated
8 metal within a dielectric material.
- 1 2. The method of claim 1 wherein providing the first metal layer
2 comprises providing a copper roll, and electroplating the metal comprises electroplating
3 additional copper.
- 1 3. The method of claim 2 further comprising creating a pattern of
2 holes in the first metal layer to define a lead frame comprising a diepad portion separated
3 from a pin portion.
- 1 4. The method of claim 3 wherein creating the pattern of holes
2 comprises etching completely through the first metal layer.
- 1 5. The method of claim 3 wherein creating the pattern of holes
2 comprises stamping completely through the first metal layer.
- 1 6. The method of claim 1 wherein the electroplating forms a QFN
2 package pin portion exposed following encapsulation.
- 1 7. The method of claim 6 wherein the electroplating forms a diepad
2 portion exposed following encapsulation..
- 1 8. The method of claim 1 wherein electroplating the metal forms a
2 raised feature on an upper side of a diepad of a power-type package selected from the
3 group consisting of TO-247, TO-220, DPAK, D2PAK, SO-x, and power BGA, for
4 ensuring even spreading of adhesive and resulting uniform attitude of a die placed attached
5 to the upper surface.

1 9. A method of fabricating a lead frame for a semiconductor device
2 package, the method comprising:
3 providing a first layer;
4 patterning a first mask over the first layer to reveal first exposed regions;
5 electroplating a first metal over the first layer in the first exposed regions;
6 patterning a second mask over the first mask to reveal second exposed
7 regions;
8 electroplating a second metal over the first mask in the second exposed
9 regions;
10 removing the first and second masks; and
11 encapsulating at least a portion of the first metal and the second metal
12 within dielectric material.

1 10. The method of claim 9 wherein the first metal and the second metal
2 are the same.

1 11. The method of claim 9 wherein:
2 patterning the first mask comprises patterning a negative photoresist mask;
3 and
4 patterning the second mask comprises patterning a negative photoresist
5 mask.

1 12. The method of claim 11 wherein removing the negative and positive
2 photoresist masks defines a lead frame comprising a diepad portion and a pin portion, the
3 method further comprising:
4 encapsulating the lead frame within a plastic package body; and
5 separating the first metal from the first layer, wherein the first exposed
6 regions correspond to a pin portion exposed on a surface of the package body.

1 13. The method of claim 12 wherein the lead frame is encapsulated
2 within a cell of a mold, such that individual packages are singulated upon separation of the
3 first metal from the first layer.

1 14. The method of claim 12 further comprising:

2 forming an etch stop layer over the first metal prior to forming the second
3 metal;

4 etching a portion of the first metal revealed by separation from the first
5 layer to form a cavity; and

6 introducing additional dielectric material within the cavity.

1 15. The method of claim 14 wherein forming the etch stop layer
2 comprises electroplating a metal different from the first and second metals within the first
3 exposed regions.

1 16. A lead frame for semiconductor device package, the lead frame
2 comprising:
3 a diepad comprising a metal;
4 a pin separate from the diepad; and
5 an electroplated raised feature comprising the metal, formed on at least one
6 of the diepad and the pin.

1 17. The lead frame of claim 16 wherein the raised feature comprises a
2 QFN package pin portion extending to a surface of the package.

1 18. The lead frame of claim 17 further comprising a second raised
2 feature comprising a portion of the diepad extending to the package surface.

1 19. The lead frame of claim 16 wherein the raised feature is located on
2 an upper surface of the diepad for ensuring even spreading of adhesive and resulting
3 uniform attitude of a die placed attached to the upper surface.

1 20. The lead frame of claim 16 wherein the raised feature comprises a
2 stud on the pin for elevating a power ball grid array (BGA) package above a surface.

1 21. The lead frame of claim 16 wherein a perimeter of the diepad
2 exhibits a serpentine shape.

1 22. The lead frame of claim 16 wherein the pin lies between the diepad
2 and an outer pin.

1 23. The lead frame of claim 22 wherein the raised feature comprises an
2 additional thickness of the outer pin, such that the outer pin is taller than the pin.

1 24. A method of fabricating a metal lead frame, the method comprising:
2 patterning a negative photoresist mask over a substrate;
3 electroplating raised portions of a copper lead frame within regions
4 exposed by the negative photoresist mask;
5 patterning a positive photoresist mask over the negative photoresist mask
6 and the raised copper portions;
7 electroplating diepad and pin portions of the copper lead frame within
8 regions exposed by the positive photoresist mask;
9 removing the negative and positive photoresist masks;
10 attaching a die to the diepad;
11 encapsulating the die and lead frame within plastic; and
12 separating the raised copper portions and the plastic from the substrate.

1 25. The method of claim 24 further comprising singulating the
2 encapsulated die and lead frame from adjacent packages by sawing.

1 26. The method of claim 25 wherein:
2 the die and lead frame are encapsulated within a cell of a surrounding mold;
3 and
4 separation of the raised copper portions and the plastic from the substrate is
5 accomplished by chemical etching, resulting in singulation of the encapsulated die and
6 lead frame from adjacent packages.

1 27. A method of fabricating a lead frame for a power ball grid array
2 (BGA) semiconductor device package, the method comprising:
3 providing a first metal layer including a pin portion;
4 patterning a mask over the first metal layer to reveal an exposed region on
5 the pin portion;
6 electroplating a metal over the exposed region to form a raised pin feature;
7 and
8 removing the mask.

1 28. The method of claim 27 further comprising:
2 providing a PC board bearing a solder ball; and
3 placing the raised pin feature into contact with a PC board, such that a body
4 of the power BGA package is elevated above the PC board in contact with the solder ball
5 and preserving a rounded shape of the solder ball.